



Optimization of Fdsoi Mosfet by using ground plane and bi axial strain

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Condition: New. Publisher/Verlag: LAP Lambert Academic Publishing | Concept of ground plane and strained silicon , design of Fdsoi Mosfet and optimization for leakage & driving current | Continued miniaturization of bulk silicon CMOS transistors is being limited by degrading short channel effects. However, these techniques are rapidly approaching material and process limits. Alternate transistor architectures such as the planar ultra-thin body (UTB) FET and double-gate MOSFET may be necessary to continue gate length scaling down to the sub-10nm regime but these structures incorporate with complex quantum physical effects. In this work the optimization and design of advanced FD SOI MOSFET structure has been done. For the optimization, concept of strained silicon, to enhance the current driving capability, and ground plane (GP), to reduce the leakage, have been deployed. Design of conventional FD SOI MOSFET, strained FD SOI MOSFET and strained GPS/GPB FD SOI MOSFET has been made at two technology nodes, 25nm and 32 nm. Device design and simulation of the above structures has been carried out using the ATLAS framework of SILVACO TCAD Tool. By the use of GP, leakage has been reduced in the conventional FD SOI MOSFET but the down side is that drive current has also been...



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