

Conception D Un Routeur Pour Les Architectures Reseaux Mono-Puce 3D (Paperback)



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Reviews

A very awesome ebook with perfect and lucid explanations. I could possibly comprehend every thing using this written e pdf. I am happy to explain how this is basically the best ebook i have got read inside my personal life and may be he very best book for ever.
(Mr. Santa Rath)

CONCEPTION D UN ROUTEUR POUR LES ARCHITECTURES RESEAUX MONO-PUCE 3D (PAPERBACK)



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Omniscriptum, 2015. Paperback. Condition: New. Language: French . Brand New Book ***** Print on Demand *****.Les interconnexions globales representent aujourd'hui un probleme dans la conception des systemes multiprocesseur sur puce (MPSoC pour Multiprocessor System-on-Chip) de haute performance. Les chercheurs des systemes embarques sont a la recherche des solutions des architectures de communications on-chip a faible cout materiel, grande fiabilite et predictibilite. Une des solutions en vue prevoit l'utilisation des reseaux d'interconnexions bases sur l'echange de paquets de donnees, appeles aussi Networks-on-Chip (NoCs). Il pourrait a terme apporter des solutions au niveau de la conception et des performances pour faire face a la complexite des systemes sur puces de grande dimension. C'est dans ce cadre que s'inscrit notre travail. En effet, il s'agit de modeliser, concevoir et valider un routeur a QoS pour une architecture NoC 3D predefinie. Deux modelisations de ce routeur ont ete realisees. L'une dans le langage VHDL au niveau RTL (Register Transfer Level) et l'autre dans le langage SystemC au niveau dit TLM-T (Transaction Level Modeling with Time). La validation du fonctionnement de l'architecture du routeur est proposee dans un reseau sur puce a topologie 3D-Mesh.



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