



Analysis and Improvement of Virtex-4 Block RAM Built-In Self-Test

By Brooks Garrison

LAP Lambert Acad. Publ. Nov 2010, 2010. Taschenbuch. Book Condition: Neu. 220x151x14 mm. Neuware - A reliable method for testing embedded memories within Virtex-4 and Virtex-5 Field-Programmable Gate Arrays (FPGAs) is needed by the current FPGA community. A method for testing the Virtex-4 embedded Block Random Access Memories (RAMs) using built-In Self-Test(BIST) was initially proposed by Daniel Milton in Built-In Self-Test of Configurable Memory Resources in Field-Programmable Gate-Arrays. However, this method was found to have deficiencies in practical application. Several corrections and improvements are made to this proposed approach, which improves overall BIST generation and execution time. A method for testing the Virtex-5 FPGA Block RAMs is proposed and the suggested configuration settings are described. Four Test Pattern Generators (TPGs) are proposed to implement the BIST, which will consist of 16 configuration bit files. 120 pp. Englisch.



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